Essential Course Information	
Course title	LABORATORY OF DIGITAL DEVICES
Degree Course title	PHYSICS
ECTS	6
Compulsory attendance	YES
Course teaching language	ENGLISH

Teacher	Saverio Simone	Saverio.Simone@uniba.it

ECTS Details	Disciplinary area	SSD	ECTS
	Characterizing	FIS/01	6

Time management and teaching activity type	Period	Year	Lesson type
	Ist semester	first	Lessons (24h) Laboratory (45h)

Time management	Total hours	In-class/in-lab study hours	Out-of-class study hours
		69	

Course calendar	Starting date	Ending date
	01.10.2020	18.12.2020

Syllabus	
Prerequisites	**Basic Analog Electronics , transistor MOS-FET and BJT**
Expected learning outcomes (according to Dublin Descriptors)	• *Knowledge and understanding:* knowledge of fundamentals of digital electronics and logic design of combinatorial and sequential circuits • *Applying knowledge and understanding:* knowledge of professional electronic CAD for logic design and simulation of digital circuits . Design and test of logical circuit to solve real problem in physics , industrial , medical and environmental fields. • *Making judgements:* Ability to analyze a problem and to propose the most appropriate electronic (circuit and technology) solution. • *Transferable communication skills:* Ability to work in a group and to develop strategies for problem solving by comparing with colleagues and teachers. • *Lifelong learning skills:* Ability to consult bibliographic material, databases and material on internet.

Course contents summary	
Detailed syllabus	**Number Systems and Conversion.** **Boolean Algebra.** **Appendix CMOS gates.** Analog and digital signals. Binary numbers. Number systems conversion. Binary variables and true or false logic. Logic functions symbols, truth tables and timing diagrams: gates AND , OR, NOT, XOR, NAND and NOR. Electrical circuits to implement logic functions: MOS and BJT transistor as switches. Totem-pole configuration . CMOS structure for NAND and NOT gates. CMOS and TTL logic families. Definition of logical levels and noise margins. Features of the logic gates: fan-out, propagation time, the rise and fall times. Examples of datasheets for integrated circuits SSI : 74LS00, 74HCT00, 74LS04,74HCT04. **Boolean algebra and Applications.** **Multi-level Gate circuits NAND and NOR .** **Application of Boolean Algebra Minterm and Maxterm.** **Karnaugh Maps.** Axiomatic definition Boolean algebra. fundamental theorems and proofs. Boolean functions. Analysis of Boolean functions and their representation as logic circuits. Complement of Boolean functions. The logic functions using NAND or NOR gates . Standard forms of Boolean functions. Transformation of a Boolean function in standard form. Examples of realization of Boolean functions by means of logic gates. Process of synthesis of Boolean functions. Minimization of Boolean functions; Method of Karnaugh maps; Maps with 3 and 4 variables. Minimum form of a Boolean function, as sum of products or product of sums expressions. Condition "don't care". Arithmetic functions: binary numbers addition and subtraction. Circuits half adder and full adder, carry-look-ahead. **Combinatorial Circuit design using gates;** **Multiplexers, Decoders, and Programmable Logic devices** Introduction to combinational logic circuits. External control of logic function using gates . Open Collector gates and wired logic. Tri-state gates and bus transmission of data, examples of datasheets for integrated 74LS125 and 74LS240. Multi-levels logical circuits and propagation delay: static and dynamic hazard. Procedures for the design of logic circuits: multiplexer, demultiplexer / Date Selector, Decoder and programmable circuits, Decoder BCD to seven segments, Encoder with priority. Codes: BCD, Gray, Excess3. Programmable devices: ROM, PLD, PROM, PAL .

	Field Programmable Gate Array (FPGA) : Structure and Hardware description logic language (Verilog). **Sequential circuits : Latches and Flip-Flops ; Register and counters .** Sequential circuits definition. Analysis of asynchronous sequential circuits . Latch Set /Reset . Synchronous sequential circuits. S-R Flip Flop . JK Flip-Flop and JK Master-Slave. D type Flip-flop and T type. Edge-triggered flip-flop. Registers (examples: datasheet for 74LS373 and 74LS374). Shift-register. FIFO and RAM memories. Asynchronous Counters. **Analysis of Clocked Sequential circuits** Characteristics equations of flip-flops. Analysis of synchronous sequential circuits . Table of States and States Graph . Design of Binary Counter circuits with T and D Flip Flop. **Laboratory experiments** Synthesis, simulation and implementation of combinational and sequential circuits : - Propagation delay measurement for NAND gates; - Design and simulation of digital circuits using PSPICE CAD; Design and Simulation of : -A 2 Bit Comparator; -A Circuit for the data transmission on a 3-State bus; -A Display using a Decoder BCD-seven segments; -A Decoder project by programming a PLD GAL16V8 ,with the OrCAD PLD program including simulation in /out; -A Decimal 2 digit Asynchronous Counter; -A 4 bit synchronous counter using D and T Flip Flop ; -FPGA Circuits Design and Simulation with VERILOG and ISE; Exercises : decoder BCD to 7 segments and TIMER.
Books	C. H. Roth , L. Kinney; Cengage Learning " Fundamentals of logic designs " ; Millman-Grabel; Ed. Mc Graw Hill " Microelettronics "; OrCAD Pspice , ORCADPLD tutorial , datasheet of electronic components (ex. http://www.alldatasheet.com/) .
Notes	Selected chapters
Teaching methods	Classroom lessons / tutorials, supported by video projector and with the help of networked PCs. CAD design in laboratories in groups of max. 2 students with the realization and testing of digital circuits
Assessment of final mark	Laboratory test of circuit, design and simulation. Oral examination
Evaluation criteria	The student **knows** basic logical circuits and methodologies for the analysis and synthesis of combinatorial and sequential logic circuits; **knows how** to design and simulate combinatorial and sequential circuits using electronic CAD;

	knows how to identify and implement the logical circuit that solves problems of applicative nature, also through group discussions or discussions with the teacher ; **know how** to write a laboratory report; **know how** to present the results of an experiment effectively in written and oral form;.
Other	